

# Risc-V Assignment Results

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The code can be found:

<https://gitfront.io/r/user-7552191/CVQXPMnSq3uo/Simplified-RISC-V-processor/>

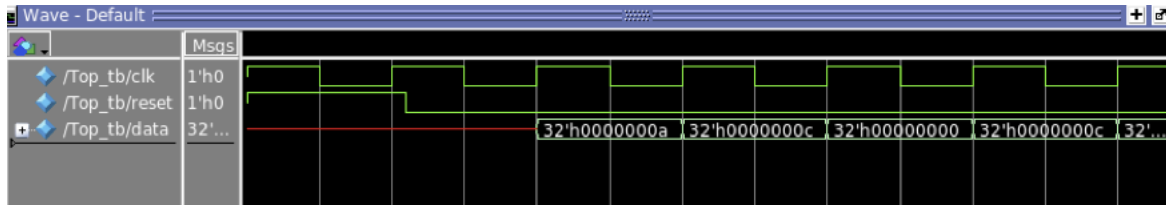


Figure 1:simulation waveform

# Register	0: 00000000	# Data Memory	0: 0000000a
# Register	1: 00000000	# Data Memory	1: xxxxxxxx
# Register	2: 00000000	# Data Memory	2: xxxxxxxx
# Register	3: 00000000	# Data Memory	3: xxxxxxxx
# Register	4: 00000000	# Data Memory	4: xxxxxxxx
# Register	5: 00000006	# Data Memory	5: xxxxxxxx
# Register	6: 00000006	# Data Memory	6: xxxxxxxx
# Register	7: 00000000	# Data Memory	7: xxxxxxxx
# Register	8: 00000000	# Data Memory	8: xxxxxxxx
# Register	9: 00000000	# Data Memory	9: xxxxxxxx
# Register	10: 0000000c	# Data Memory	10: xxxxxxxx
# Register	11: 0000000a	# Data Memory	11: xxxxxxxx
# Register	12: 00000000	# Data Memory	12: 0000000c
# Register	13: 0000000c	# Data Memory	13: xxxxxxxx
# Register	14: ffffffff4	# Data Memory	14: xxxxxxxx
# Register	15: 00000016	# Data Memory	15: xxxxxxxx
# Register	16: 00000000	# Data Memory	16: xxxxxxxx
# Register	17: 00000000	# Data Memory	17: xxxxxxxx
# Register	18: 00000000	# Data Memory	18: xxxxxxxx
# Register	19: 00000000	# Data Memory	19: xxxxxxxx
# Register	20: 0000000c	# Data Memory	20: ffffffff4
# Register	21: 00000000	# Data Memory	21: xxxxxxxx
# Register	22: 00000000	# Data Memory	22: xxxxxxxx
# Register	23: 00000000	# Data Memory	23: xxxxxxxx
# Register	24: 00000000	# Data Memory	24: xxxxxxxx
# Register	25: 00000001	# Data Memory	25: xxxxxxxx
# Register	26: 00000000		

Figure 2:Registers and data memory after simulation

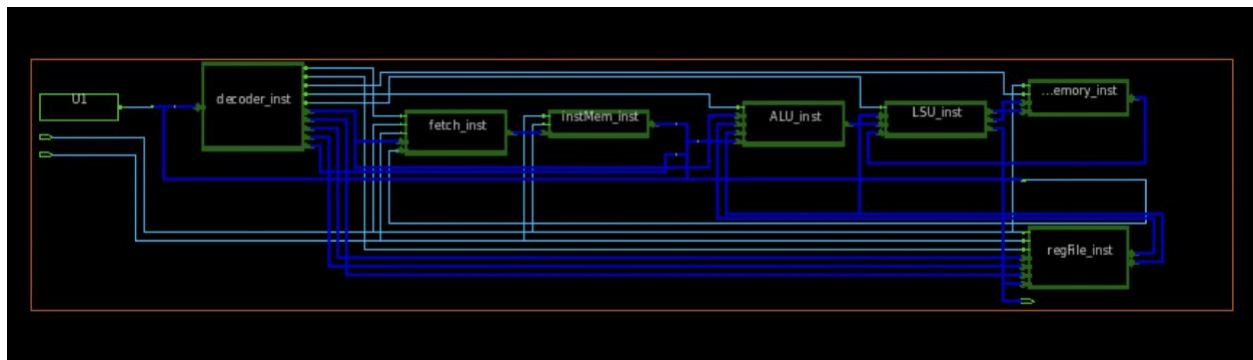


Figure 3: Schematic Compile\_result

## Area Report

```
*****
Report : area
Design : Top
Version: 0-2018.06-SP5-5
Date   : Sun May  8 19:57:40 2022
*****

Library(s) Used:

  GF22FDX SC8T 104CPP_BASE CSC20L TT 0P90V 0P00V 0P00V 0P00V 25C (File: /eda work/GF_Library/
libraries/dbs/20lvt_dbs/GF22FDX_SC8T_104CPP_BASE_CSC20L_TT_0P90V_0P00V_0P00V_0P00V_25C_ccs.db)

Number of ports:          1106
Number of nets:           11120
Number of cells:          10010
Number of combinational cells: 6847
Number of sequential cells: 3151
Number of macros/black boxes: 0
Number of buf/inv:        217
Number of references:      8

Combinational area:       3243.136000
Buf/Inv area:             63.631358
Noncombinational area:    5215.974506
Macro/Black Box area:     0.000000
Net Interconnect area:    undefined (No wire load specified)

Total cell area:          8459.110506
Total area:               undefined
```

Figure 4:Area Report

## Power Report

```
Global Operating Voltage = 0.9
Power-specific unit information :
  Voltage Units = 1V
  Capacitance Units = 1.000000ff
  Time Units = lps
  Dynamic Power Units = 1mW (derived from V,C,T units)
  Leakage Power Units = 1uW

Cell Internal Power = 11.9594 mW (93%)
Net Switching Power = 894.2804 uW (7%)
-----
Total Dynamic Power = 12.8537 mW (100%)
Cell Leakage Power = 21.0903 uW
```

Power Group	Internal Power	Switching Power	Leakage Power	Total Power	( % )	Attrs
io_pad	0.0000	0.0000	0.0000	0.0000	( 0.00%)	
memory	0.0000	0.0000	0.0000	0.0000	( 0.00%)	
black_box	0.0000	0.0000	0.0000	0.0000	( 0.00%)	
clock_network	0.0000	0.0000	0.0000	0.0000	( 0.00%)	
register	11.9275	2.1374e-07	12.7354	11.9402	( 92.74%)	
sequential	0.0000	0.0000	0.1580	1.5796e-04	( 0.00%)	
combinational	3.1514e-02	0.8943	8.1968	0.9340	( 7.25%)	
Total	11.9590 mW	0.8943 mW	21.0902 uW	12.8744 mW		
1						

Figure 5: Power Report

Timing Report

data arrival time			705.80
clock clk (rise edge)	780.00		780.00
clock network delay (ideal)	1.00		781.00
clock uncertainty	-1.80		779.20
fetch_inst/pc_reg[15]/CLK (SC8T_DFFRQX1_CSC20L)	0.00		779.20
library setup time	-21.30		757.90
data required time			757.90
-----			
data required time			757.90
data arrival time			-705.80
-----			
slack (MET)			52.10

1

Figure 6: Timing Report

PnR results

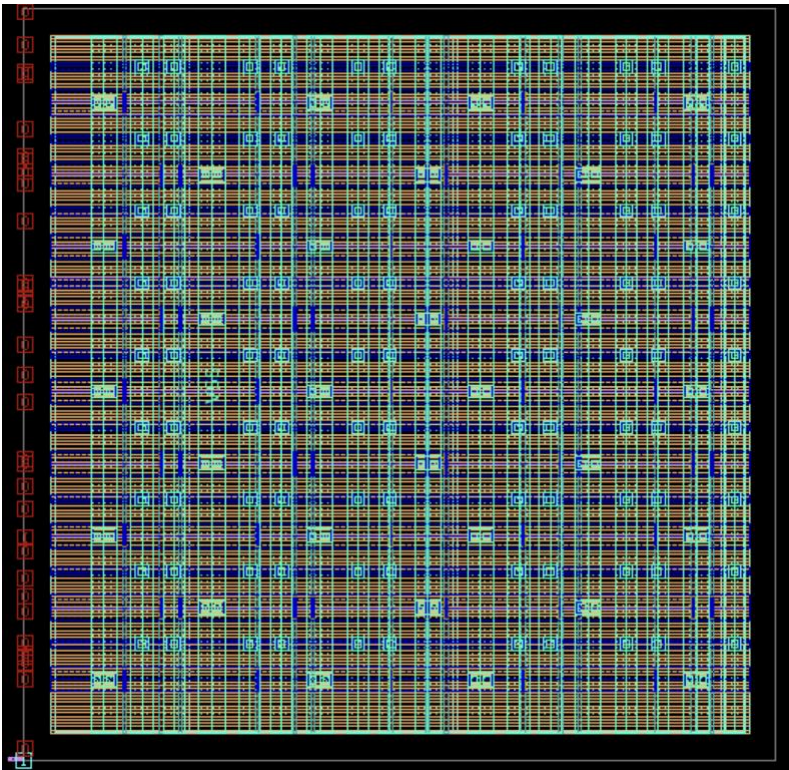


Figure 7: Final Chip Design

```
Lib Top_lib /eda_work/Aaron_Tekleab/PnR/PNR_sorted/icc2/work/Top_lib tech current
- 0 Top.design May-09-15:52
+> 0 Top/chip_finish.design May-09-16:26 current
- 0 Top/clock_opt_cts.design May-09-16:04
- 0 Top/clock_opt_opto.design May-09-16:12
- 0 Top/init_design.design May-09-15:52
- 0 Top/place_opt.design May-09-15:54
- 0 Top/route_auto.design May-09-16:14
- 0 Top/route_opt.design May-09-16:25
```

8

```
icc2_shell>
```