ID pattern-based Counter Project

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Digital ASIC Design

Project Problem

1) You need to design a counter that counts according to the pattern of your student ID from LSD to MSD
    a. It needs to have up_dn input to reverse the counting pattern
    b. You need to parametrize it so that you can change the pattern from the TB
2) Build a TB that shows the full operation of the counter
3) Synthesize it and generate timing, are and power reports
4) Perform PNR and generate reports and screenshot showing the critical path

Solution

The following section shows the screenshot of the results of the counter design starting from simulation of the RTL code, synthesis using dc_shell, and followed placement and routing using ICC2_shell. Different reports for all stages are provided alongside a short brief description.
The default pattern is from LSD to MSD. However, this can be altered using the en_up input port. Moreover, the provided ID can also be changed in testbench since they are parameterized.

Results Screenshots

Figure 1 shows the simulation of the counter deployed. The counting pattern can be changed via the en_up input port. The default pattern is from LSD to MSD. And the numbers have been parameterized thus the user can input the needed 9-digit ID number. The default ID input is: 100043374.

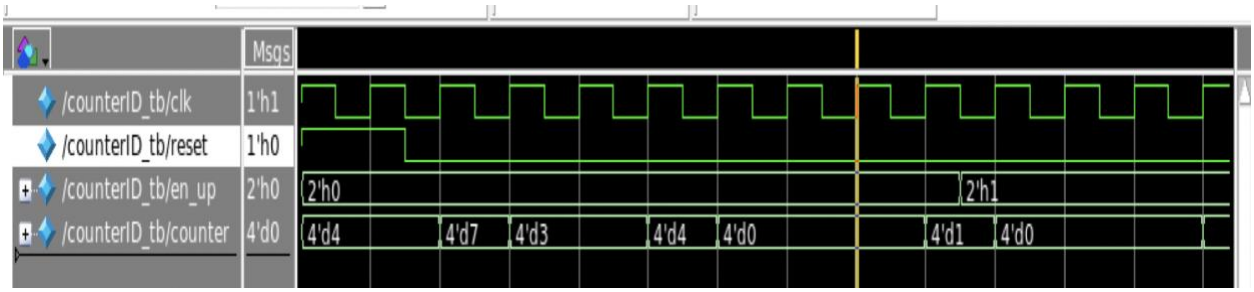

Figure 1:Simulation Result

Figure 2 shows the synthesized netlist using dc_shell software.

Figure 2: Synthesis Result

Figure 3 shows the area report of the synthesized netlist shown in figure 2. According to the report the total area required is 14.44352 square units.

```
****************************************
Report : area
Design : counterID
Version: O-2018.06-SP5-5
Date   : Mon May 16 00:15:13 2022
****************************************

Library(s) Used:

    GF22FDX_SC8T_104CPP_BASE_CSC20L_TT_0P90V_0P00V_0P00V_0P00V_25C (File: /eda_w
ork/GF_Library/libraries/dbs/20lvt_dbs/GF22FDX_SC8T_104CPP_BASE_CSC20L_TT_0P90V_
0P00V_0P00V_0P00V_25C_ccs.db)

Number of ports:                           8
Number of nets:                           39
Number of cells:                          35
Number of combinational cells:            31
Number of sequential cells:                4
Number of macros/black boxes:              0
Number of buf/inv:                         7
Number of references:                     15

Combinational area:                 8.320000
Buf/Inv area:                       0.931840
Noncombinational area:              6.123520
Macro/Black Box area:               0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                   14.443520
Total area:                 undefined
1
```

Figure 3: Synthesis Area Report

Figure 4 shows the power report of the synthesized netlist. The internal, switching and leakage power can be seen in the report. The total power is reported to be 70.209 µW.

```
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1uW


  Cell Internal Power  =  50.4152 uW   (72%)
  Net Switching Power  =  19.7443 uW   (28%)
                         ---------
Total Dynamic Power    =  70.1595 uW  (100%)

Cell Leakage Power     =  49.2076 nW


                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %
   )  Attrs
--------------------------------------------------------------------------------
-----------
io_pad             0.0000           0.0000            0.0000           0.0000  (   0.
00%)
memory             0.0000           0.0000            0.0000           0.0000  (   0.
00%)
black_box          0.0000           0.0000            0.0000           0.0000  (   0.
00%)
clock_network      0.0000           0.0000            0.0000           0.0000  (   0.
00%)
register       3.1985e-02       1.0835e-03        1.9329e-02       3.3087e-02  (  47.
13%)
sequential         0.0000           0.0000            0.0000           0.0000  (   0.
00%)
combinational  1.8431e-02       1.8661e-02        2.9863e-02       3.7121e-02  (  52.
87%)
--------------------------------------------------------------------------------
-----------
Total          5.0415e-02 mW     1.9744e-02 mW     4.9193e-02 uW     7.0209e-02 mW
1
```

Figure 4: Synthesis Power Report

The resources are also reported in figure 5.

```
****************************************
Report : resources
Design : counterID
Version: O-2018.06-SP5-5
Date   : Mon May 16 00:17:27 2022
****************************************


Resource Report for this hierarchy in file
        /eda_work/Aaron_Tekleab/counterProject/synProject/counterID.sv
===============================================================================
| Cell           | Module         | Parameters | Contained Operations       |
===============================================================================
| sub_x_1        | DW01_dec       | width=4    | sub_77 (counterID.sv:77)   |
| add_x_2        | DW01_inc       | width=4    | add_87 (counterID.sv:87)   |
===============================================================================


Implementation Report
===============================================================================================
|                    |                  | Current            | Set            |
| Cell               | Module           | Implementation     | Implementation |
===============================================================================================
| sub_x_1            | DW01_dec         | apparch (area)     |                |
| add_x_2            | DW01_inc         | apparch (area)     |                |
===============================================================================================

1
```

Figure 5: Synthesis Resources Report

The clock period initially provided is 200 units. And it had a positive slack of 26.81 units.

```
  Startpoint: N_reg[0] (rising edge-triggered flip-flop clocked by clk)
  Endpoint: N_reg[3] (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock clk (rise edge)                    0.00       0.00
  clock network delay (ideal)              1.00       1.00
  N_reg[0]/CLK (SC8T_DFFQX1_CSC20L)        0.00       1.00 r
  N_reg[0]/Q (SC8T_DFFQX1_CSC20L)         43.00      44.00 f
  U41/Z (SC8T_NR2X1_MR_CSC20L)            15.30      59.30 r
  U46/Z (SC8T_AN2X1_MR_CSC20L)            26.37      85.67 r
  U34/Z (SC8T_AOI211X0P5_CSC20L)          25.14     110.81 f
  U57/Z (SC8T_ND2IAX1_MR_CSC20L)          15.06     125.88 r
  U36/Z (SC8T_OAI21X1_CSC20L)             13.32     139.19 f
  U58/Z (SC8T_AOI32X1_MR_CSC20L)          13.58     152.78 r
  U59/Z (SC8T_ND2X1_MR_CSC20L)            10.11     162.89 f
  N_reg[3]/D (SC8T_DFFQX1_CSC20L)          0.00     162.89 f
  data arrival time                                 162.89

  clock clk (rise edge)                  200.00     200.00
  clock network delay (ideal)              1.00     201.00
  clock uncertainty                       -1.80     199.20
  N_reg[3]/CLK (SC8T_DFFQX1_CSC20L)        0.00     199.20 r
  library setup time                      -9.50     189.70
  data required time                                189.70
  -----------------------------------------------------------
  data required time                                189.70
  data arrival time                                -162.89
  -----------------------------------------------------------
  slack (MET)                                       26.81
```

Figure 6: Synthesis Timing Report

The following figures 7 and 8 show the placement and routing of the designed counter. The red pins show the input-output ports. While the building cells are shown zoomed in figure 8.

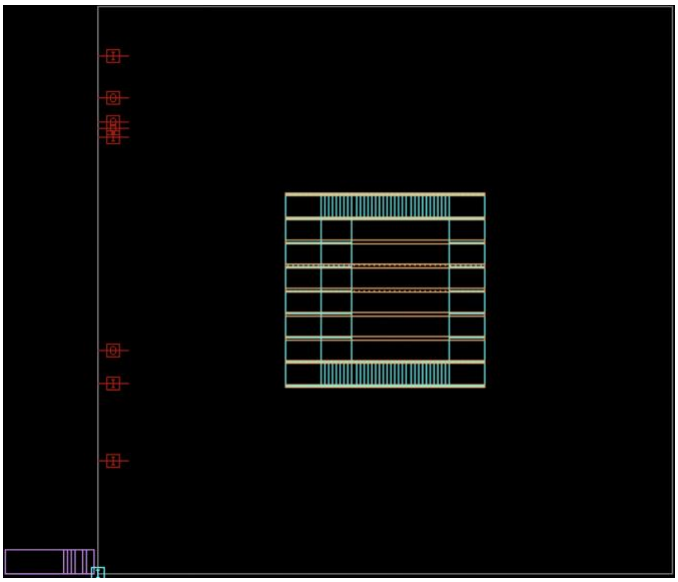

Figure 7: PnR...1

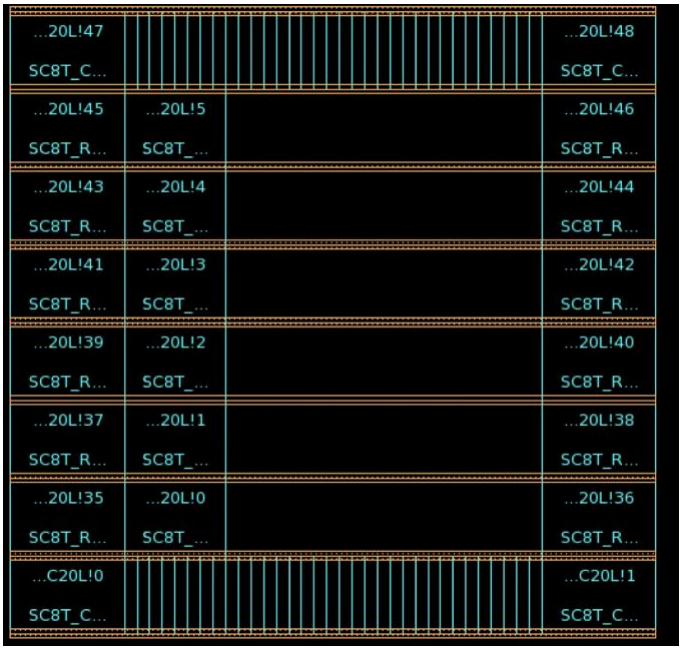

Figure 8: PnR...2

After the PnR process, the timing report resulted into -116 units time slack. Therefore, additional 150 timing units were added, and the process was performed again resulting into +33 timing units slack. The screenshot of the timing report is shown below in figure 9. The worst timing path (critical path) is shown below i.e., the data required time is 368.71 time. units while the data arrival time is 330.35 units results into +33 slack time units.

```
Startpoint: N_reg[0] (rising edge-triggered flip-flop clocked by clk
Endpoint: N_reg[3] (rising edge-triggered flip-flop clocked by clk)
Mode: func
Corner: ssg0p72vm40c_FuncRCmax
Scenario: func::ssg0p72vm40c_FuncRCmax
Path Group: reg2reg
Path Type: max

Point                                          Incr      Path
-----------------------------------------------------------------------
clock clk (rise edge)                          0.00      0.00
clock network delay (propagated)              19.39     19.39

N_reg[0]/CLK (SC8T_DFFQX1_CSC20L)              0.00     19.39 r
N_reg[0]/Q (SC8T_DFFQX1_CSC20L)               97.39    116.78 f
U41/Z (SC8T_NR2X1_MR_CSC20L)                  28.34    145.12 r
U46/Z (SC8T_AN2X1_MR_CSC20L)                  49.17    194.30 r
U34/Z (SC8T_AOI211X0P5_CSC20L)                40.57    234.86 f
U57/Z (SC8T_ND2IAX1_MR_CSC20L)                28.97    263.84 r
U36/Z (SC8T_OAI21X1_CSC20L)                   22.07    285.91 f
U58/Z (SC8T_AOI32X1_MR_CSC20L)                25.22    311.12 r
U59/Z (SC8T_ND2X1_MR_CSC20L)                  19.23    330.35 f
N_reg[3]/D (SC8T_DFFQX1_CSC20L)                0.00    330.35 f
data arrival time                                      330.35

clock clk (rise edge)                        350.00    350.00
clock network delay (propagated)              14.72    364.72
clock reconvergence pessimism                  4.59    369.32
N_reg[3]/CLK (SC8T_DFFQX1_CSC20L)              0.00    369.32 r
clock uncertainty                             -1.80    367.52
library setup time                            -3.81    363.70
data required time                                     363.71
-----------------------------------------------------------------------
data required time                                     363.71
data arrival time                                     -330.35
-----------------------------------------------------------------------
slack (MET)                                            33.36
```

Figure 9: Timing Report after PnR